INTRODUCTION TO THE Am9513 SYSTEM TIMING CONTROLLER

ADVANCED MICRO DEVICES

APPLICATION BRIEF
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OVERVIEW

The Am9513 System Timing Controller is a processor-oriented support device designed to enhance system capability with respect to counting and timing operations. Functionally, a single STC contains an internal oscillator with associated circuitry plus five general-purpose 16-bit counters. Each counter is supported by independent control circuitry that allows it to be individually configured.

The internal frequency source is scaled so that five different internal frequencies are available for selection as inputs for any of the counters. A selected internal frequency may also be brought out for direct use in other parts of the system.

Each counter can be programmed to count up or count down and to count in binary or in BCD. Sixteen counting sources are available for each counter and input polarity is also individually selectable. Gating functions allow direct hardware and software control of count accumulation. Several combinations of output configurations and polarities are available. Control of the count modulo is provided by allowing automatic repetitive initialization of the counter from a control register. Any of the counters may be internally concatenated with an adjacent counter.

Counters 1 and 2, in addition to their use in the same ways as counters 3, 4 and 5, may also be configured to operate as a 24-hour real-time clock. Auxiliary alarm registers on counters 1 and 2 may be used to detect the presence of a specific counter value.

The internal control elements of the STC may be accessed by the host processor in several ways. Random access to any element for either reading or writing is easily accomplished using an addressing command before each data transfer. Alternatively, automatic consecutive access can be used without command intervention to simplify many operating procedures.

Block Diagram

The general block diagram shown in Figure 1 indicates the Am9513 STC interface signals and the basic flow of information. Internal control lines and the internal data bus have been omitted. The control and data registers are all connected to a common internal 16-bit bus. The external bus may be 8 or 16-bits wide; in the 8-bit mode the internal 16-bit information is multiplexed at the chip interface.

The STC is addressed by the external system as two locations: a control port and a data port. The control port provides direct access to the Status and Command registers. The data port is used to communicate with all other internal locations. The Status register reflects the state of the counter outputs to help the host processor coordinate STC activities under software control. The Command register is used to initiate and control the operation of each counter plus the access methods available for the other locations.

The internal oscillator provides a convenient source of frequencies for use as counter inputs. Its oscillating frequency is controlled at the X1, X2 inputs by an external reactive network such as a

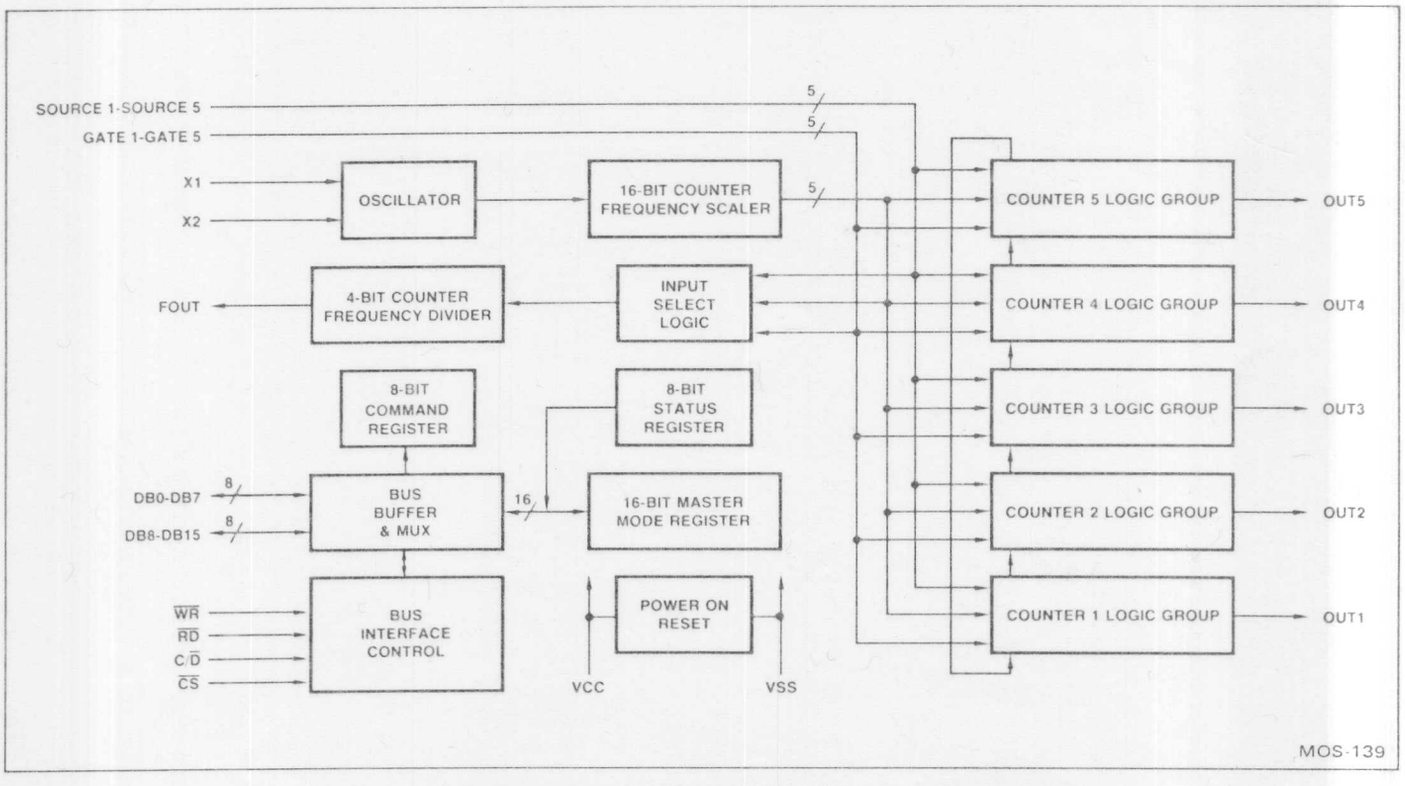

Figure 1. Am9513 General Block Diagram.

crystal. The oscillator output is divided by the Frequency Scaler to provide several sub-frequencies. One of the scaled frequencies or one-of-ten interface input signals may be selected for division before coming out of the chip at the FOUT interface pin.

The Master Mode register controls the overall chip options that are not included in the Counter Mode registers. It selects the frequency scaling mode, the time-of-day functions, the FOUT divider ratio, etc. Each of the five general counters is 16 bits long and is independently supported by registers and control logic that allow it to be used in many different operating modes. See Figures 2 and 3. The input select logic steers one of 16 sources to the counter input. The counter control logic interprets the Mode selections to control several counter functions, including up/down, binary/BCD and count gating. The Load register is used to automatically re-initialize the counter to any predefined value, thus controlling the effective length (modulo value) of the counter. The Hold register may also be used for automatic modulo control and in addition it is used to save intermediate counter values so that the host processor can gain access to that information without interfering with the count process. Output control logic, including a toggling bit, is configured by a field in the Counter Mode register and allows several types of output waveforms and polarities to be selected.

All five counters have the same basic control logic and control registers. Counters 1 and 2 have additional alarm registers and comparators associated with them, plus the extra logic necessary for operating in a 24-hour time-of-day mode. For real-time operation the time-of-day logic will accept 50Hz or 60Hz or 100Hz input frequencies.

Notice that each general counter has a single dedicated output pin. It may be turned off when the output is not of interest, or may be configured in a variety of ways to drive interrupt controllers or darlington buffers or bus drivers, etc. The counter inputs, on the other hand, are specifically not dedicated to any given interface line. Considerable versatility is available for configuring both the input and the gating of individual counters. This not only permits dynamic reassignment of inputs under software control, but also allows multiple counters to use a single input, and allows a single gate pin to control more than one counter. Indeed, a single pin can be the gate for one counter and, at the same time, the count source for another.

Figure 4 summarizes the 40 interface signals for the Am9513. The port addressing and information transfers are specified by the C/$\overline{D}$ control line in conjunction with the $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ inputs. Sixteen pins are used for the data bus; in the 8-bit interface mode

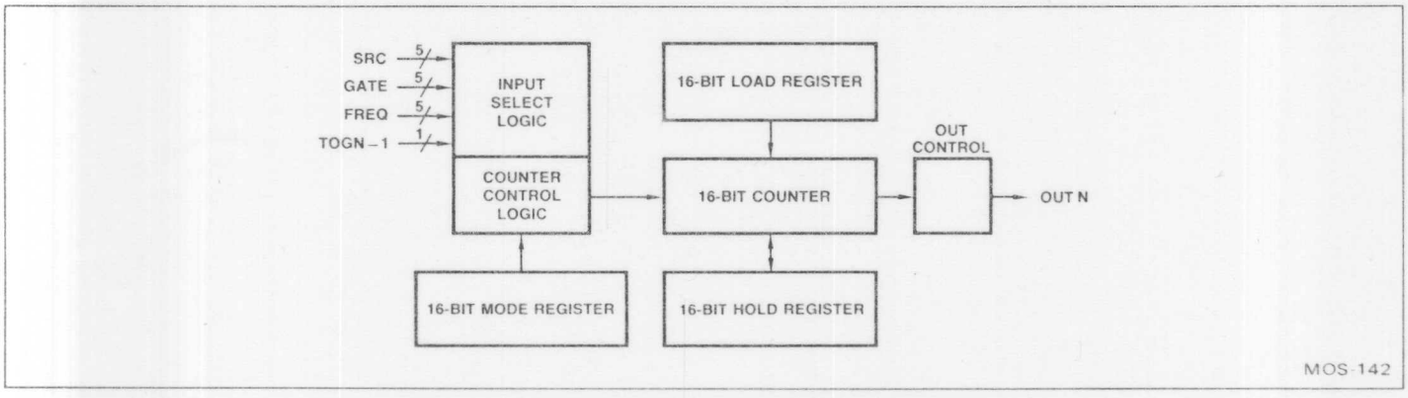

Figure 2. Counter Groups 3, 4 and 5 Block Diagram.

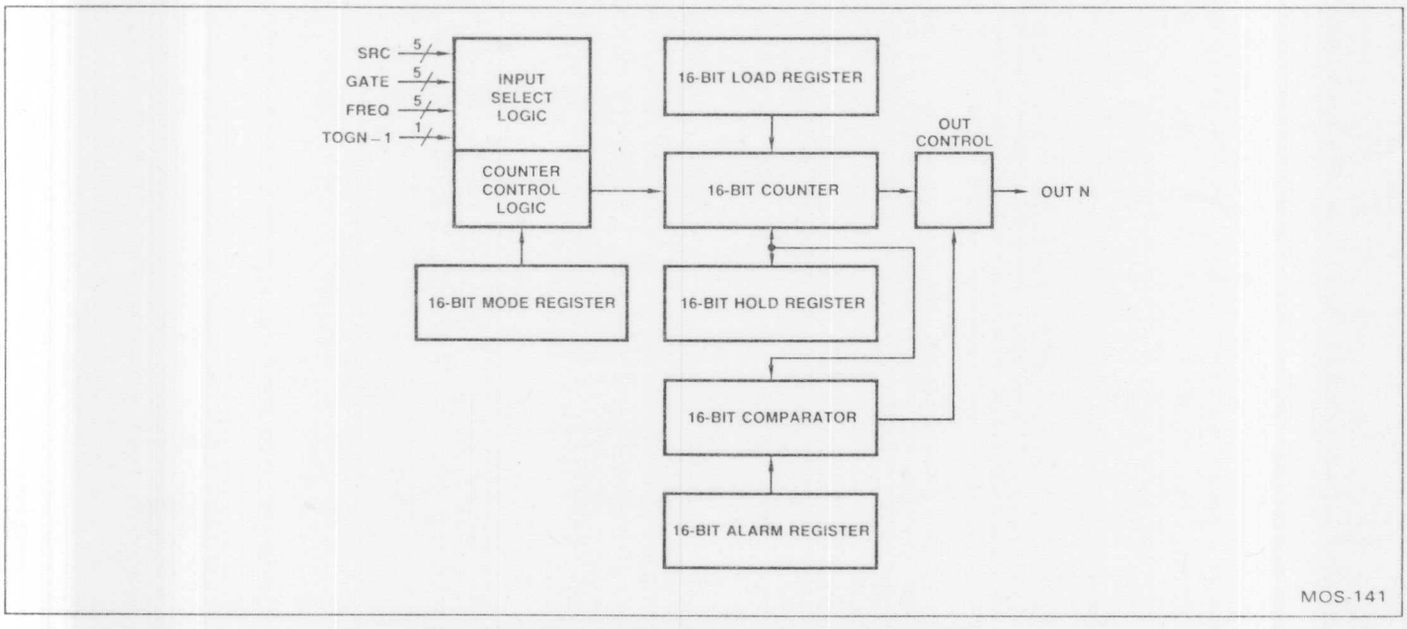

Figure 3. Counter Groups 1 and 2 Block Diagram.

only the low-order eight pins transfer information. Any of the SRC pins may be directed to any of the counters as a counting source. The GATE pins are dual-purpose and may be used for both gating and as counting sources.

Signal	Abbreviation	Type	Pins
+5 Volts	VCC	Power	1
Ground	VSS	Power	1
Crystal	X1, X2	Input	2
Read	$\overline{RD}$	Input	1
Write	$\overline{WR}$	Input	1
Chip Select	$\overline{CS}$	Input	1
Control/Data	C/$\overline{D}$	Input	1
Source N	SRC	Input	5
Gate N	GATE	Input	5
Data Bus	DB	I/O	16
Frequency Out	FOUT	Output	1
Out N	OUT	Output	5

Figure 4. Interface Signal Summary.

Figure 5 summarizes all the internal registers, counters and comparators. Most are accessible, in one form or another, by the host processor for both reading and writing.

Name	Bit Size	Quantity
Output Control Bit	1	5
FOUT Divider Counter	4	1
Data Pointer Counter	5	1
Status Register	6	1
Command Register	8	1
Frequency Scaling Counter	16	1
Master Mode Register	16	1
Alarm Register	16	2
Comparator	16	2
Counter Mode Register	16	5
Counter Load Register	16	5
Counter Hold Register	16	5
General Counter	16	5

Figure 5. Control Element Summary.

Master Mode Control

The 16-bit Master Mode (MM) register is used to control all those optional internal activities that are not controlled by the individual Counter Mode registers. These controls include frequency scaling, FOUT divider, time-of-day operation, comparator enabling, data bus width and access sequencing. The MM bit assignments are shown in Figure 6.

Bits MM0 and MM1 control the time-of-day (TOD) option on counters 1 and 2. When TOD is disabled, the special logic for decoding hours, minutes and seconds is bypassed and the counters will perform in the same way as counters 3, 4 and 5. When TOD is enabled it can operate in real-time from 50Hz, 60Hz or 100Hz inputs.

Bits MM2 and MM3 control the two comparators associated with counters 1 and 2. When enabled, a comparator output is steered to the OUT pin in place of the normal counter output. In TOD mode, either comparator may be used individually; when both are enabled their function is concatenated, requiring a full 32-bit compare in order to generate an output at OUT 2.

Bits MM4 through MM7 specify which of the 15 inputs will be selected for the FOUT divider. The 16th combination (all zeros) turns FOUT off and puts it in a high impedance state. One of the internal frequencies derived from the scaled oscillator will often be chosen and the FOUT signal may then be used as a system clock.

Bits MM8 through MM11 specify the dividing ratio for the 4-bit FOUT divider. This counter divides the source (selected by bits MM4 through MM7) by some integer value from 1 through 16 and then passes the result to the FOUT buffer.

Bit MM12 enables or disables the FOUT signal. When disabled, FOUT is a low impedance to ground; for a three-state high impedance condition the FOUT source field should be used. After power-up or reset, FOUT is enabled.

Bit MM13 controls the data bus interface multiplexer to configure the part for an 8-bit or 16-bit external bus. The internal bus is always 16 bits wide. After power-up or a software reset, the unit is in its 8-bit mode. A single command may be used to convert into the 16-bit mode.

Bit MM14 controls the Data Pointer logic to enable or disable the automatic increment function. This permits the host processor to sequentially read or write groups of data registers or to repetitively read or write at a single location.

Bit MM15 controls the counting configuration of the Frequency Scaler. The 16-bit Scaler can be setup to divide the oscillator frequency in binary or in BCD steps.

Counter Mode Control

A 16-bit Counter Mode (CM) register is associated with each of the five general-purpose counters. They independently control the operating and configuration options for each general counter. These controls include output configuration, count control, count source and polarity selection, and gating control. The CM bit assignments are shown in Figure 7.

Bits CM0 through CM2 control the output configuration. The OUT pin may be off and in a high impedance state, or off with a low impedance to ground. The output waveform may be a terminal count pulse, indicating that the count has reached zero, or may be the output of a flip-flop that is toggled by the terminal count pulse. In either case, the signal may be specified as active high or active low.

Bits CM3 through CM7 control various parameters affecting the counting process. CM3 defines up or down counting. CM4 controls binary or BCD counting. CM5 controls the single-cycle/continuous count mode, to simplify digital one-shot operation when desired. CM6 allows the automatic initialization of the counter to occur from the Load register only or from both the Load and Hold registers. The CM7 bit is conditioned by the gating control field and may be used to enable/disable the retriggering capability or to allow selection of the loading source for automatic initialization.

Bits CM8 through CM12 control the count source selection and polarity. CM12 indicates active high or active low polarity for the input specified by CM8 through CM11. Sixteen candidates are available for selection as counting sources and include the five internal frequencies derived from the oscillator, the five SRC pins, the five GATE pins and the toggle output from the adjacent counter.

Bits CM13 through CM15 control the various gating options available. When the specified gate is active, counting can proceed if the counter has been armed; an inactive gate disables counting. Active gating can be level controlled or can be initiated by a pulse.